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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/894,862	06/27/2001	Michael Lee	020174-005400US	3693

20350 7590 02/04/2005

TOWNSEND AND TOWNSEND AND CREW, LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO, CA 94111-3834

EXAMINER	
PHAN, THAI Q	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 02/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/894,862	LEE ET AL.	
	Examiner	Art Unit	
	Thai Q. Phan	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-57* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 1/2/02 and 7/08/02
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to patent application S/N: 09/894,862. Claims 1-57 are pending in this Action.

Information Disclosure Statement

The information disclosure statements filed Jan. 02, 2002 and 07/08/2002 have been considered.

Drawings

The drawings were received on 02/04/2002. These drawings are acceptable.

Specification

Applicants are required to provide current status of the related and cross-references as cited in the specification.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Quake et al, US patent application no. US 2002/0037499 A1.

. As per claim 1, Quake discloses a method and system for designing and fabricating microfluidic device with feature limitations very similar to the claimed invention. According to Quake, the microfluidic device design method includes steps

placing a plurality of circuit components on a design schematic for the circuit, wherein the device component has associated functional information ([0021]-[0024], for example),

connecting the components together to implement the design circuit as in the last claimed step. Quake does not expressly disclose the claimed "symbol" for component part as claimed.

Practitioner in the art at the time of the invention was made would have found it obvious that a component of the circuit model in the design process has a symbol representing for circuit function such as R for resistance, C for capacitance, AND, OR logic gates, etc.

As per claim 2, Quake discloses a multilayered structure for the circuit component ("Chip Fabrication", [303]-[0313], for example).

As per claim 3, Quake discloses materials such as elastomeric material for nanoscale device or microfluidic structure ([0369]).

As per claim 4, Quake discloses a multi-channel chip design for fluid flow channel, control channel as claimed (Figs. 14, 15, [0313]-[0324]).

As per claims 5-7, Quake discloses the logic gates as claimed for chip design and fabrication.

As per claim 8, Quake discloses a plurality of design components with symbols for chip layout and fabrication.

As per claims 9-13, Quake discloses a plurality of fluid channels and control channels for component interconnection.

As per claim 14, Quake discloses microfluidic circuit structure for logic operation as claimed.

As per claim 15, Quake discloses a method and system for designing and fabricating microfluidic device with feature limitations very similar to the claimed invention. According to Quake, the microfluidic device design method includes steps

placing a plurality of component elements with circuit component model on a design schematic for the circuit, wherein the device component has associated functional information ([0021]-[0024], for example),

connecting the components together to implement the design circuit as in the last claimed step. Quake does not expressly disclose the claimed "symbol" for component part as claimed.

Practitioner in the art at the time of the invention was made would have found it obvious that a component with functional model in the design has a symbol or a component model representing for circuit function such as R for resistance, C for capacitance, AND, OR logic gates, etc.

As per claims 16 and 17, Quake disclosure would include element as claimed [0028].

As per claims 18-23, Quake discloses the design methodology includes generating a plurality of channel connected elements, fluid channels, and control channel to implement the design.

As per claim 24, Quake discloses a method and system for designing and fabricating microfluidic device with feature limitations very similar to the claimed invention. According to Quake, the microfluidic device design system includes means:

placing a plurality of component models from the design library for the circuit schematic, wherein the device component has associated functional information ([0021]-[0024], for example),

connecting the components together to implement the design circuit as in the last claimed step. Quake does not expressly disclose the claimed "symbol" for component part as claimed.

Practitioner in the art at the time of the invention was made would have found it obvious that a component in the design circuit has a symbol representing for circuit function such as R for resistance, C for capacitance, AND, OR logic gates, etc.

As per claims 25 and 26, Quake discloses a multilayered structure for the circuit component ("Chip Fabrication", [303]-[0313], for example). Such layer structure would be for device parameters such as size, depth, etc.

As per claim 27, Quake discloses a multi-channel chip design for fluid flow channel, control channel as claimed (Figs. 14, 15, [0313]-[0324]).

As per claim 28, Quake discloses materials such as elastomeric material for nanoscale device or microfluidic structure ([0369]).

As per claims 29-31, Quake discloses circuit design environment, which would obviously include computerized means for circuit design and layout as claimed.

As per claims 32-33 and 43-44, Quake discloses a computer program product implemented in the design system for designing and fabricating microfluidic device with feature limitations very similar to the claimed invention. According to Quake, the microfluidic device design program product includes means:

placing a plurality of component models from the design library for the circuit schematic, wherein the device component has associated functional information ([0021]-[0024], for example),

connecting the components together to implement the design circuit as in the last claimed step. Quake does not expressly disclose the claimed "symbol" for component part as claimed.

Practitioner in the art at the time of the invention was made would have found it obvious that a component in the design circuit has a symbol (model) representing for circuit function such as R for resistance, C for capacitance, AND, OR logic gates, etc.

As per claims 34-37, 45 and 52, Quake discloses the claimed limitations for the microfluidic circuit design.

As per claims 38, 42, 46-49, 51, and 57, Quake discloses programming languages being used in the design process. They would include the claimed standard languages for the design process.

As per claims 39, 50, 53, 54, and 55-56, Quake discloses a synthesis system for designing and fabricating microfluidic device with feature limitations very similar to the claimed invention. According to Quake, the microfluidic device design system includes means:

Storing a plurality of device components for the circuit design,

placing a plurality of component models from the design library for the circuit schematic, wherein the device component has associated functional information ([0021]-[0024], for example),

connecting the components together to implement the design circuit as in the last claimed step.

And analyzing the design and testing the design circuit based on design connectivity and functional model [0049], for example. Quake does not expressly disclose the claimed "symbol" for component part as claimed.

Practitioner in the art at the time of the invention was made would have found it obvious that a component in the design circuit has a symbol representing for circuit function such as R for resistance, C for capacitance, AND, OR logic gates, etc.

As per claims 40-41, Quake discloses the limitations as claimed for the design process.

Conclusion

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. US patent no. 6,500,323 B1, issued to Chow et al, on Dec. 2002

2. US patent no. 6,569,382 B1, issued to Edman et al, on May 2003

3. US patent no. 6,637,463 B1, issued to Lei et al, on Oct. 2003

4. US patent application publication no. US 2002/0197603 A1, issued to Chow et al, on Dec. 2002

5. US patent application publication no. US 2002/0108097 A1, issued to Harris et al, on Aug. 2002

6. US patent application publication no. US 2004/0096960 A1, issued to Burd Mehta et al, on May 2004

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thai Q. Phan whose telephone number is 571-272-3783.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean Homere can be reached on 571-272-3780. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

3. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Feb. 02, 2005

Thai Phan
Patent Examiner
Art Unit 2128